IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Attorney Docket: CY-0006

In re application of: **JIN et al.**

Serial No.: **09/405,945**

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APPELLANT'S BRIEF

Timing of Appeal Brief and Fees Required Pursuant to 37 C.F.R. 1.192(a)(b)

This brief is in furtherance of the Notice of Appeal, filed in this case on July 25, 2003 and is due September 25, 2003.

The fees required under 37 C.F.R. 1.17(c), and any fees for a petition for extension of time for filing this brief are dealt with in the accompanying Transmittal of Appeal Brief.

Certificate of Mailing/Transmission (37 C.F.R. 1.8(a))

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Appeal Brief Items Pursuant to 37 C.F.R. 1.192(c)

This brief contains the following items under the headings, and in the order set forth below.

1. Real Party in Interest
2. Related Appeals and Interferences
3. Status of Claims
4. Status of Amendments
5. Summary of Invention
6. Issues
7. Grouping of Claims
8. Argument
9. Appendix

1. Real Party in Interest

The patent application on appeal is owned, by assignment, by Cypress Semiconductor Corporation, a Delaware Corporation, having offices at 3901 North First Street, San Jose, CA 95134.

2. Related Appeals and Interferences

There are no other appeals or interferences related to, or that may be affected by a decision of the Board of Patent Appeals and Interferences (the Board) on this appeal.

3. Status of Claims

The status of all claims is set forth below:

Claims cancelled: Claims 15 and 20.

Claims allowed: None.

Claims rejected: Claims 1-14 and 16-19.

The claims on appeal are claims 1-14 and 16-19.

4. Status of Amendments

Amendments were submitted after the final rejection, but not entered by the Examiner.

These amendments would have reduced the issues on appeal by incorporating the limitations of dependent claims into base claims.

In particular, the limitations of dependent claim 2 were incorporated into base claim 1, the limitations of dependent claim 14 were incorporated into base claim 12, and limitations of dependent claim 19 were incorporated into base claim 18. This would have eliminated claims 2 and 12 from appeal.

5. Summary of Invention

The invention of claim 1 is directed toward a method of forming a contact hole through a first insulating layer (e.g., FIG. 1, item **106**, FIG. 2C and the Specification, page 13, lines 6-14 and page 13, line 21 to page 14, line 3; FIG. 3, item **306**, FIG. 4C and the Specification, page 16, lines 16-21; FIG. 5, item **522**, FIG. 6K and the Specification, page 24, line 3 to page 25, line 3). The etched contact hole is self-aligned with respect to a transistor gate (e.g., the Specification, page 4, lines 8-10, page 24, Lines 3-4). The transistor gate has a gate length of less than 0.2 microns (e.g., the Specification, page 27, Table 1, where a "Poly CD Final" value is 0.160 microns, and page 9, lines 15-17). The contact hole is formed without forming an etch stop liner (e.g., FIGS. 2C and 2D, and the Specification, page 12, lines 2-5, page 13, lines 15 to 20; page 14, lines 1-3; FIGS. 4B and 4C, and the Specification, page 15, lines 17 to 22, page 16, lines 22-23; FIG. 6K and the Specification, page 20, line 2, page 26, lines 9-10).

The invention of claim 2 includes the various steps described for claim 1, but adds that forming a contact hole includes reactive plasma etching (e.g., the Specification, page 13, line 13; page 24, line 5 to page 25, lines 5-7) through a first insulating layer comprising silicon dioxide (e.g., the Specification, page 11, line 23 to page 12, line 1).

The invention of claim 3 includes the various steps described for claim 1, but adds that forming a contact hole includes reactive plasma etching (e.g., the Specification, page 13, line 13; page 24, line 5 to page 25, lines 5-7). Further, such etching is through a first insulating layer comprising silicon dioxide. The silicon dioxide has a phosphorous dopant concentration that is greater than 5% by weight (e.g., the Specification, page 12, lines 5-11; page 21, lines 16-17).

The invention of claim 12 is a method that includes etching a contact hole through a first insulating layer (e.g., FIG. 1, item **106**, FIG. 2C and the Specification, page 13, lines 6-14 and page 13, line 21 to page 14, line 3; FIG. 3, item **306**, FIG. 4C and the Specification, page 16, lines 16-21; FIG. 5, item **522**, FIG. 6K and the Specification, page 24, line 3 to page 25, line 3). The first insulating layer comprises doped silicon dioxide (e.g., the Specification, page 12, lines

5-11; page 20, lines 13-14). The contact hole is self-aligned with respect to a conductive structure (e.g., the Specification, page 4, lines 8-10; FIG. 2C; FIG. 4C; FIG. 6K, and the Specification, page 24, Lines 3-4). The conductive structure is formed over a substrate and includes insulating sidewalls (e.g., FIGS. 2A to 2D, items **204** and **206**, and the Specification, page 11, lines 16-17; FIGS. 4A to 4D, items **402**-1 and **404**-1, and the Specification, page 14, line 24 to page 15, line 1; FIGS. 6D to 6K, items **618**-1 and **618**-2, and the Specification, page 19, line 24 to page 20, line 1). Etching is performed with particular etch selectivity parameters. The etch selectivity between the first insulating layer and the sidewall is greater than ten to one (e.g., the Specification, page 25, lines 7-8). The etch selectivity between the first insulating layer and substrate is greater than one hundred to one (e.g., the Specification, page 25, lines 18-20).

The invention of claim 13 includes the various steps described for claim 12, but adds that the insulating sidewalls comprise silicon nitride (e.g., the Specification, page 11, line 19; page 19, lines 14-19).

The invention of claim 14 includes the various steps described for claim 12, but adds forming the first insulating layer to comprise silicon dioxide having a phosphorous concentration that is greater than 5% by weight (e.g., the Specification, page 12, lines 5-11; page 21, lines 16-17).

The invention of claim 17 includes the various steps described for claim 12, but adds forming a hard etch mask comprising an insulating material over the first insulating layer (e.g., FIG. 6I to 6K, item **622**, and the Specification, page 23, lines 2-10) and forming a contact hole includes etching through the first insulating layer with a selectivity between the first insulating layer and the hard etch mask that is greater than fifty to one (e.g., FIG. 6K, the Specification, page 25, lines 13-15). The hard etch mask comprises silicon dioxide (e.g., the Specification, page 22, lines 8-9). The first insulating layer comprises phosphorous doped silicon dioxide (e.g., the Specification, page 20, line 13).

The invention of claim 18 is a method that includes forming a hard mask comprising substantially undoped silicate glass (e.g., FIGS. 6I to 6K, item **622**, and the Specification, page 23, lines 2-10). The hard mask is formed over an insulating layer comprising doped silicon dioxide (e.g., FIG. 6G, the Specification, page 22, lines 6-7). The hard mask has openings over a contact hole location (e.g., the Specification, page 23, lines 11-12). A contact hole is formed at the contact hole location through the first insulating layer (e.g., FIG. 6K and the Specification, page 24, line 4 to page 25, line 3). The contact hole is formed between conducting structures that are separated from one another by less than 0.4 microns (e.g., the Specification, page 27, Table 1, where a "Poly Pitch" has a value of 0.460 microns and a "Poly CD Final" value is 0.160 microns, thus a separation distance is 0.460-0.160 = 0.300 microns). The conducting structures have sidewalls (e.g., FIGS. 6D to 6K, items **618**-1 and **618**-2, and the Specification, page 19, line 24 to page 20, line 1). The contact hole is formed without forming a protective liner over the conducting structures (e.g., FIG. 6K and the Specification, page 20, line 2, page 26, lines 9-10).

The invention of claim 19 includes the various steps described for claim 18, but adds that the insulating layer comprises silicon dioxide having a concentration of phosphorous dopant that is greater than 5% by weight (e.g., the Specification, page 21, lines 16-17) and the sidewalls comprise silicon nitride (e.g., the Specification, page 19, lines 14-19).

6. Issues

The issues presented for review are set forth below.

Issue 1 - Whether claim 1 is patentable over *Hsue* (U.S. Patent No. 5,378,654) in view of *Chang et al.* (U.S. Patent No. 5,893,740).

Issue 2 - Whether claim 2 is patentable over *Hsue* in view of *Chang et al.*, and further in view of *Nulty et al.* (U.S. Patent No. 5,468,342).

Issue 3 - Whether claims 4-11 are patentable over *Hsue* in view of *Chang et al.*, and further in view of *Nulty et al.*

Issue 4 - Whether claim 3 is patentable over *Hsue* in view of *Chang et al.* further in view of *Figura et al.* (U.S. Patent No. 5,661,064).

Issue 5 - Whether claims 12 is patentable over *Hsue* in view of *Nulty et al.*

Issue 6 - Whether claim 13 is patentable over *Hsue* in view of *Nulty et al.* further in view of *Chang et al.*

Issue 7 - Whether claim 14 is patentable over *Hsue* in view of *Nulty et al.* further in view of *Figura et al.*

Issue 8 - Whether claims 16 and 17 are patentable over *Hsue* in view of *Nulty et al.* further in view of *Atsushi* (Japanese Publication No. 10-223897) and further in view of *Ploessl et al.* (U.S. Patent No. 5,907,771).

Issue 9 - Whether claim 18 is patentable over U.S. Patent No. 5,376,562 (*Fitch et al.*) in view of U.S. Patent No. 5,776,834 (*Avanzino et al.*).

Issue 10 - Whether claim 19 is patentable over *Fitch et al.* in view of *Avanzino et al.* further in view of *Figura et al.*

7. Grouping of Claims

Claim 1 stands or falls alone.

Claim 2 stands or falls alone.

Claim 3 stand or fall together.

Claims 4-11 stand or fall together.

Claims 12-13 and 16 stand or fall together.

Claim 14 stands or falls alone.

Claim 17 stands or falls alone.

Claim 18 stands or falls alone.

Claim 19 stands or falls alone.

8. Argument

8(i) Rejections Under 35 U.S.C. §112, First Paragraph

No claims were rejected on these grounds.

8(ii) Rejections Under 35 U.S.C. §112, Second Paragraph

No claims were rejected on these grounds.

8(iii) Rejections Under 35 U.S.C. §102

No claims were rejected on these grounds.

8(iv) Rejections Under 35 U.S.C. §103

The following arguments explain why the claim groups indicated in Section 7 are believed to be separately patentable.

Issue 1 - Whether claim 1 is patentable over *Hsue* (U.S. Patent No. 5,378,654) in view of *Chang et al.* (U.S. Patent No. 5,893,740).

Independent claim 1 recites a method that includes forming a contact hole through a first insulating layer that is self-aligned with respect to a transistor gate. The transistor gate has a gate length of less than 0.2 microns. Further, the contact hole is formed without a contact hole etch stop liner.

The rejection of claim 1 admits that that while *Hsue* shows a self-aligned contact etch, *Hsue* does not show a transistor with a gate length of less than 0.2 microns.[1] To show a transistor with a gate length of less than 0.2 microns, the rejection proposes modifying *Hsue* according to *Chang et al.*, which teaches a short channel field effect transistor with a gate length of 0.1 microns.

The motivation for the combination relied upon by the rejection was stated in the Final Office Action.

> It would have been obvious... to modify Hsue by using a transistor with gate length of less than 0.2 microns as taught by Chang for the purpose of increasing switching speed.[2]

As is well established, a prima facie case of obviousness requires there must be some suggestion or motivation to combine reference teachings. Further, a rejection may not selectively choose favorable aspects of a reference while ignoring contrary teachings. In particular:

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[1] See the Final Office Action dated 3/25/03 (Paper 15), Page 3, Lines 1-2.
[2] See *Id.*, Page 3, Lines 10-12.

> [P]rior art references... must be read as a whole and consideration must be given where the references diverge and teach away from the claimed invention...[3]

Similarly, if a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.[4]

The combination of *Hsue* in view of *Chang et al.* renders the reference *Hsue* unsatisfactory for its intended purpose. Accordingly, the rejection has not presented the necessary motivation required to establish a prima facie case of obviousness.

The reference *Hsue* teaches a self-aligned contact process. As shown in *Hsue*, a self-aligned contact is a contact formed adjacent to a conductive structure. The contact remains electrically isolated from the contact by insulating sidewalls and a top insulating layer.[5] *Hsue* emphasizes this by indicating that such a top insulating layer (e.g., cap layer) is conventionally kept thick:

> A conventional Self-Aligned Contact (SAC) process uses **a thick cap layer over** polysilicon gate structures. The cap layer is composed silicon dioxide material for spacer and SAC contact etching back. The process window is a trade off with increased step height.[6]

Chang et al. is not compatible with the *Hsue* process relied upon by the rejection. *Chang et al.* teaches a short channel field effect transistor that does not include an insulating or dielectric layer formed on the top of the gate.[7] *Chang et al.* intentionally removes any cap (or similar) layer formed on a gate:

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[3] Azko N.V. v. United States Intl' Trade Comm'n, 1 USPQ 2d 1241, 1246 (Fed. Cir. 1986).
[4] In re Gordon, 221 USPQ 1125 (Fed. Cir. 1984).
[5] See *Hsue*, FIG. 1F, where a conductive contact 28 is isolated from gates 12, by insulating sidewalls 18 and top (cap) insulating layer 14.
[6] *Id.*, Col. 1, Lines 9-13, emphasis added.
[7] See *Chang et al.*, FIGS. 1(b) and 3(b), which show a silicide layer formed on the top of the gate electrode 13 and 23. No dielectric layer is formed on the gate.

> [D]eposit a layer of dielectric material, and remove horizontal surfaces of such layer...[8]

Thus, incorporating the transistor of *Chang et al.* into the *Hsue* process would defeat the SAC process of *Hsue*, as no structure would exist to prevent the gate from being exposed when the contact hole is etched. That is, there is no structure over the top of the gate that would insulate the conductive gate from a subsequently formed conductive contact.

Even if the above divergent teachings are improperly ignored, and only a gate of *Chang et al.* is incorporated into the teachings of *Hsue*, such a modification would render the device of *Hsue* unsatisfactory for its intended purpose. *Hsue* appears to be directed to relatively large transistor sizes. In particular, the disclosed embodiment of *Hsue* appears to show a self-aligned contact process for a gate length of 0.8 μm – nearly four times the size limit of the claimed invention.[9] As noted, the rejection proposes incorporating the much smaller gate size of *Chang et al.* into the process of *Hsue*:

> Chang is relied upon to teach forming a gate structure having a transistor gate length of less than 0.2 μm...[10]

However, *Chang et al.* clearly indicates that simply utilizing such small gate sizes does not produce devices of sufficient functionality:

> As the channel length (L_{gate}) becomes shorter and shorter, short channel effects tend to occur. Thus, how to suppress the short channel effects is very important in today's technology.[11]

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[8] *Id.*, Col. 3, Lines 28-29 and Col. 4, Lines 34-33.

[9] See *Hsue*, FIGS. 2A and 2B, and accompanying descriptions in Col. 3 and 4. In particular, Col. 3, Lines 65-67 indicate a polysilicon/polycide layer 42 has a thickness of about 3,000 Å. Col. 4, Lines 22-24 indicate that a silicon dioxide layer 46 thickness is preferably about 2,500 Å. FIGS. 2A and 2B thus appear to be drawn close to scale. A measurement of the gate length in FIGS. 2A and 2B yields a length of about 8,000 Å, which equals 0.8 μm. Appellants' claim 1 limitations recite a gate of length less than 0.2 μm.

[10] See the Final Office Action dated 3/25/03 (Paper 15), Page 12, Lines 3-4.

Thus, simply incorporating a smaller size gate into a transistor, without any additional structures, would result in a device that suffers from short channel effects – precisely what is sought to be corrected in *Chang et al.*

Chang et al. explicitly teaches away from simply reducing a gate size by teaching particular features to address short channel effects: ion implantation doses to form short channel source and drain regions[12], as well as a tilt ion implantation step that necessarily relies on a silicide layer on the top of the gate, a silicide layer on the substrate, as well as a particular sidewall on the gate.[13] However, as noted above, such structures are not suitable for a self-aligned contact process. In particular, the top of the gate is not covered with a cap insulating layer.

Thus, if the rejection relies on simply incorporating a short channel gate size of *Chang et al.* into the process of *Hsue*, such a device would not address short channel effects, and thus make the resulting transistor unsuitable for operation. Said in another way, one skilled in the art would be led away from such a combination by the explicit teachings of *Chang et al.*, which indicates such a combination (i.e., simply inserting a smaller gate size while ignoring the other teachings of the reference) creates a transistor with undesirable short channel effects.

Because sufficient suggestion or motivation for the proposed combination is not present in the reference, a prima facie case of obviousness has not been established for the rejection of claim 1. Accordingly, Appellant respectfully seeks reversal of the rejection of claim 1.

Issue 2 - Whether claim 2 is patentable over *Hsue* in view of *Chang et al.*, and further in view of *Nulty et al.* (U.S. Patent No. 5,468,342).

The invention of claim 2 includes the limitation of claim 1, but further adds that forming the contact hole includes reactive plasma etching through the first insulating layer, where the

[11] *Chang et al.*, Col. 1, Lines 11-15.
[12] See *Id.*, Col. 3, Lines 21-27.
[13] See *Id.*, Col. 3, Lines 49-54 and FIGS. 1(c) and 3(c), which notes that silicide layers 17 on a gate and substrate serve as a mask for a tilt (LATI) implant. As shown in FIG. 1(c), impurities are implanted through a sidewall.

first insulating layer comprises non-densified doped silicon dioxide.

As noted above, claim 2 recites forming a contact hole through a first insulating layer comprising non-densified doped silicon dioxide. Because claim 2 depends from claim 1, such a contact hole is formed "without forming a contact hole etch stop liner".

Such a limitation is not shown or suggested by the cited combination of references.

The reference relied upon, *Hsue*, shows the formation of a contact hole. However, such a contact hole is through an un-doped silicon dioxide.[14]

The second reference relied upon, *Chang et al.*, provides no teachings regarding any contact formation, let alone the formation of a contact hole through an insulating layer.

To show a "non-densified doped silicon dioxide layer", as recited in claim 2, the rejection relies on the "Background of the Invention" set forth in *Nulty et al.*:

> Nulty teaches forming contact openings in an oxide layer (column 4, lines 21 and 22). The oxide layer may be undoped or doped, for example BPSG (borophosphosilicate glass) (column 1, lines 17-25) by reactive ion etching (column 1, lines 14-25 and column 6, lines 15-20 and 54-57, and column 7, lines 4-6 and 17-19).[15]

However, this portion of *Nulty et al.* clearly does not show, and in fact teaches away from Appellants' claim 1 limitation of "without forming a contact hole etch stop liner". *Nulty et al.* teaches an etch stop layer is included in the formation of an opening (e.g., contact opening):

> As shown, structure 404 is covered by silicon nitride etch stop layer 403.[16]

Thus, the portions of *Nulty et al.* relied upon by the rejection appear no different than Appellants' Background Art, which utilizes etch stop liners (i.e., layers) to protect a substrate.

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[14] See *Hsue*, FIGS. 1D and 1E and Col. 2, Lines 4-16, which describes forming a SAC contact opening through (undoped) SiO_2 layer 21.
[15] See the Final Office Action, dated 3/25/03, Page 3, Lines 18-21.
[16] *Nulty et al.*, Col. 3, Lines 50-51, emphasis added.

Appellants' invention overcomes such a limitation by dispensing with liners while still enabling relatively small gate length sizes (e.g., 0.2 microns or less).

Because the portions of *Nulty et al.* relied upon by the rejection shows the utilization of an etch stop layer, such a teaching thus explicitly teaches away from Appellants' claim 1 limitation of "without an etch stop liner". Alternatively, such contrary teachings would rebut any prima facie obviousness.

For all of these reasons, the rejection of claim 2 is believed to be error, and should be reversed.

Issue 3 - Whether claims 4-11 are patentable over *Hsue* in view of *Chang et al.*, and further in view of *Nulty et al.*

Claims 4-11 all depend from claim 3. Claim 3 includes the particular limitation of the first insulating layer having a phosphorous dopant concentration of greater than 5% by weight. This ground for rejection is believed to be error as the rejection has admitted the above combination does not show such a limitation:

> Hsue in view of Chang and further in view of Nulty differs in failing to teach a silicon dioxide having a concentration of phosphorous dopant that is greater than 5% by weight.[17]

Thus, because the rejection admits that the above combination does not teach limitations inherent in claims 4-11 (from claim 3), a prima facie of obvious cannot have been established for these claims based on *Hsue* in view of *Chang et al.*, further in view of *Nulty et al.*

Issue 4 - Whether claim 3 is patentable over *Hsue* in view of *Chang et al.* further in view of *Figura et al.* (U.S. Patent No. 5,661,064).

Claim 3, which depends from claim 1, recites that forming the contact hole includes

[17] See the Final Office Action, dated 3/25/03, Page 5, Lines 1-3.

etching through a layer comprising silicon oxide having a concentration of phosphorous dopant that is greater than 5% by weight.

The necessary motivation for combining *Figura et al.* with *Hsue* and *Chang et al.* to establish a prima facie case of obviousness is believed to be lacking.

The motivation relied upon for adding *Figura et al.* to the combination is set forth below.

> It would have been obvious... to modify Hsue in view of Chang by implanting silicon dioxide with a phosphorous dopant that is greater than 5% for the purposes of enhancing the conductive properties of an intrinsic insulative material such as SiO_2.[18]

This motivation is not an objective teaching from the prior art, nor is it believed to be general knowledge available to one skilled in the art. Appellants note that *Figura et al.* teaches an intrinsically insulative material having a conductivity enhancing dopant impurity provided therein.[19] *Figura et al.* never teaches enhancing the conductive properties of an intrinsic insulative material. Accordingly, the rationale relied upon is not an objective teaching from the prior art.

The rationale is not believed to be general knowledge, either. The rationale teaches a contradictory goal – increasing the conductivity of an insulating layer. As is well understood an insulating layer provides insulation by being non-conductive. Known rationales for doping an insulating layer are discussed at length in Appellants' Specification (e.g., preferential gettering and flow properties), and do not include seeking to increase the conductivity of an insulating layer.[20]

Thus, because the motivation relied upon is not from the cited reference, the rejection is improper, and should be reversed.

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[18] See the Final Office Action, dated 3/25/03, Page 5, Lines 7-10, emphasis added.
[19] See *Figura et al.*, Col. 3, Lines 18-21.
[20] See the Specification, Page 6, Line 9 to Page 7, Line 18.

Issue 5 - Whether claim 12 is patentable over *Hsue* in view of *Nulty et al.*

The invention of claim 12 is a method that includes etching a contact hole through a first insulating layer. The first insulating layer comprises doped silicon dioxide. The contact hole is self-aligned with respect to a conductive structure. The conductive structure is formed over a substrate and includes insulating sidewalls. Etching is performed with particular etch selectivity parameters. The etch selectivity between the first insulating layer and the sidewall is greater than ten to one. The etch selectivity between the first insulating layer and substrate is greater than one hundred to one.

The rationale set forth for rejecting claim 12 is set forth below.

> Since Hsue etches and uses the same method of etching a contact hole through a first insulating layer... as that of the claimed invention, then using Hsue's method would inherently result in an etch selectivity between the first insulating layer and the sidewall that is greater than ten to one, and an etch selectivity between the first insulating layer and substrate that is greater than one hundred to one.[21]

The method of etching shown in *Hsue* is clearly different than Appellants' claimed invention. Claim 12 clearly recites doped silicon dioxide. *Hsue* does not show a first insulating layer of doped silicon dioxide.[22] Thus, the cited reference does not show the same materials as Appellants' claimed invention, and so factual allegations relied upon by the rejection are not true.

Because the basis for establishing the inherency of Appellants' claim 12 limitations is based on inaccurate facts, such evidence cannot sustain a prima facie case of obviousness. Accordingly, this ground of rejection should be reversed.

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[21] See the Final Office Action, dated 3/25/03, Page 5, Line 19 to Page 6, Line 4.
[22] See *Hsue*, Col. 2, Lines 3-5 and Col. 4, Lines 19-22, which describe silicon dioxide layers 21 and 46, with no indication of doping.

Issue 6 - Whether claim 13 is patentable over *Hsue* in view of *Nulty et al.*, and further in view of *Chang et al.*

To the extent that this ground of rejection relies on the combination of *Hsue* in view of *Nulty et al.*, Appellants incorporate by reference herein the comments set forth above for **Issue 5**. Namely, that the factual allegations relied upon to establish the prima facie case of obviousness are incorrect. Thus, the "inherent" disclosure of claim 12 limitations based on such allegations has not been established.

Further, the extent that the rejection relies on combining *Chang et al.* with *Hsue*, the comments set forth above for **Issue 1** are incorporated by reference herein. Namely, that the motivation for combining *Chang et al.* with *Hsue* is lacking, thus a prima facie case of obviousness has not been established or is rebutted.

Issue 7 - Whether claim 14 is patentable over *Hsue* in view of *Nulty et al.* further in view of *Figura et al.*

To the extent that this ground of rejection relies on the combination of *Hsue* in view of *Nulty et al.*, Appellants incorporate by reference herein the comments set forth above for **Issue 5**.

Further, the extent that the rejection relies on combining *Figura et al.* with *Hsue*, the comments set forth above for **Issue 4** are incorporated by reference herein. Namely, that the motivation relied upon is not an objective teaching from the cited art or common knowledge.

Issue 8 - Whether claims 16 and 17 are patentable over *Hsue* in view of *Nulty et al.* further in view of *Atsushi* (Japanese Publication No. 10-223897) and further in view of *Ploessl et al.* (U.S. Patent No. 5,907,771).

To the extent that this ground of rejection relies on the combination of *Hsue* in view of *Nulty et al.*, Appellants incorporate by reference herein the comments set forth above for **Issue 5**.

In addition, Appellants believe claim 17 includes additional patentable limitations above and beyond claim 12.

Claim 17, which depends from claim 16, recites that a hard etch mask comprises silicon dioxide and a first insulating layer comprises phosphorous doped silicon dioxide.

To show the limitations of claim 17, the rejection proposes combining *Ploessl et al.* with *Hsue* in view of *Nulty et al.*, and further in view of *Atsushi*. However, motivation for combining *Ploessl et al.* to the reference is lacking, as the proposed modification would change the principle operation of the method and device of *Hsue*.

Hsue is directed to a self-aligned contact process. Such a process exposes a substrate by etching a dielectric layer so that a contact may be brought in contact with the substrate.[23] In very sharp contrast, *Ploessl et al.* is directed to forming a trench capacitor. Such a process etches a substrate.[24] Thus, to modify *Hsue* according to *Ploessl et al.* would change the contact etch of *Hsue* into a substrate etch – thereby changing the principal operation of *Hsue*. More particularly, using the etch of *Ploessl et al.* removes the very structure (substrate surface) necessary to form a contact in the method and device of *Hsue*.

For these reasons, the rejection of claims 16 and 17 should be reversed.

Issue 9 - Whether claim 18 is patentable over U.S. Patent No. 5,376,562 (*Fitch et al.*) in view of U.S. Patent No. 5,776,834 (*Avanzino et al.*).

A prima facie case of obviousness has not been established for claim 18, as the cited combination does not show or suggest all the limitations of claim 18.

The combination of references does not show a hard mask comprising substantially undoped silicate glass. *Fitch et al.* shows a method of forming vertical transistors that utilizes a mask of photoresist. While *Fitch et al.* shows two dielectric layers, such layers are never utilized as hard mask layers. Only photoresist is used as a mask.[25]

It is additionally noted that the term "hard mask" does not appear in the text of *Fitch et al.* Because *Fitch et al.* never shows or mentions the use of a hard mask, Appellants do not

[23] See *Hsue*, FIG. 1F, and Col. 2 Lines 25-28, which describe how a contact 28 is brought into contact with the substrate surface.
[24] See *Ploessl et al.*, FIG. 3C and Col. 4, Lines 30-39.
[25] See *Fitch et al.*, Col. 3, Line 61 to Col. 4, Line 8. In particular see Col. 4, Lines 5-9, which shows that the opening that extends through the dielectric layers 16 and 20 is self-aligned with the (photoresist) mask opening.

believe the reference can be suggestive of such a limitation.

The other reference *Avanzino et al.* is unrelated to contact hole formation, and so provides no teachings regarding masks, let alone hard masks.

Accordingly, because the combination of references fails to show all limitations of claim 18, a prima facie case of obviousness has not been established, and this ground of rejection should be reversed.

Issue 10 - Whether claim 19 is patentable over *Fitch et al.* in view of *Avanzino et al.* further in view of *Figura et al.*

To the extent that this ground of rejection relies on the combination of *Fitch et al.* in view of *Avanzino et al.*, the comments set forth above for **Issue 9** are incorporated by reference herein. Namely, the combination of references fails to show or suggest all limitations of claim 18, from which claim 19 depends.

In addition or alternatively, to the extent that the rejection relies on the motivation of "increasing the conductive properties of an intrinsic insulative material" to combine *Figura et al.* with the other references, Appellants incorporate by reference herein the comments set forth above for **Issue 4**. Namely, that such a rationale is neither an objective teaching in the prior art, or knowledge generally available to one of ordinary skill in the art.

Conclusion.

For the various reasons set forth above, Appellants' respectfully contend that a prima facie case was never established for the claims at issue. Accordingly, a reversal of all claim rejections is respectfully requested.

Respectfully Submitted,
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APPENDIX A

CLAIMS INVOLVED IN THE APPEAL

1. A method, comprising:

forming a contact hole through a first insulating layer that is self-aligned with respect to a transistor gate having a gate length less than 0.2 microns without forming a contact hole etch stop liner.

2. The method of claim 1, wherein:

forming the contact hole includes reactive plasma etching through the first insulating layer comprising non-densified doped silicon dioxide.

3. The method of claim 1, wherein:

forming the contact hole includes reactive plasma etching through the first insulating layer comprising silicon dioxide having a concentration of phosphorous dopant that is greater than 5% by weight.

4. The method of claim 3, wherein:

the reactive plasma etching includes introducing CHF_3 and $C_2H_2F_4$ into an etch chamber.

5. The method of claim 4, wherein:

the flow rate of CHF_3 is less than ten times the flow rate of $C_2H_2F_4$.

6. The method of claim 5, wherein:

the flow rate of CHF_3 is in the general range of 3-15 standard centimeter cubed per minute (sccm); and

the flow rate of $C_2H_2F_4$ is in the general range of 10-100 sccm.

7. The method of claim 3, wherein:

the reactive plasma etching includes exciting a plasma with a radio frequency power source that supplies power in the general range of 100 to 1000 Watts.

8. The method of claim 3, wherein:

the reactive plasma etching includes an etch time in the general range of 80 to 200 seconds.

9. The method of claim 3, wherein:

the contact hole is formed on a target object that is biased to an absolute value potential in the general range of 100 to 1500 Volts.

10. The method of claim 3, wherein:

the reactive plasma etching pressure is in the general range of 20-100 milliTorrs.

11. The method of claim 3, wherein:

the reactive plasma etching temperature is in the general range of 0-35 °C.

12. A method, comprising:

etching a contact hole, through a first insulating layer comprising doped silicon dioxide, that is self-aligned with respect to a conductive structure that is formed over a substrate and includes insulating sidewalls with an etch selectivity between the first insulating layer and the sidewall that is greater than ten to one, and an etch selectivity between the first insulating layer and the substrate that is greater than one hundred to one.

13. The method of claim 12, wherein:

the insulating sidewalls comprise silicon nitride.

14. The method of claim 12, further including:

forming the first insulating layer comprising a high density plasma silicon dioxide having a concentration of phosphorous dopant that is greater than 5% by weight.

15. Cancelled

16. The method of claim 12, further including:

forming a hard etch mask comprising an insulating material over the first insulating layer; and

forming the contact hole includes etching through the first insulating layer with a selectivity between the first insulating layer and the hard etch mask that is greater than fifty to one.

17. The method of claim 16, wherein:

the hard etch mask comprises silicon dioxide; and

the first insulating layer comprises phosphorous doped silicon dioxide.

18. A method, comprising:

forming a hard mask comprising substantially undoped silicate glass over an insulating layer comprising doped silicon dioxide, the hard mask having openings over a contact hole location; and

forming a contact hole at the contact hole location through the insulating layer between conducting structures separated from one another by less than 0.4 microns and having sidewalls, without forming a protective liner over the conducting structures.

19. The method of claim 18, wherein:

the insulating layer comprises silicon dioxide having a concentration of phosphorous dopant that is greater than 5% by weight; and

the sidewalls comprise silicon nitride.

20. Cancelled.